FEB 17 1992

Order this document
by MC68HC34TS/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC68HC34

Technical Summary
Dual-Port RAM Memory Unit

Introduction

The MC68HC34 dual-port RAM memory (DPM) unit enables two processors operating on separate buses to exchange data. The unit allows one processor to exchange data with the other without interfering with devices on the second processor's bus. The medium for this transfer is 256 bytes of dual-port RAM.

The DPM contains six semaphore registers that provide a means for controlling access to the dual-port RAM or any other shared resource. Interrupt registers allow the two processors to interrupt each other.

Features

- High-Speed Complementary Metal-Oxide Semiconductor (HCMOS) Structure
- Six Read/Write Semaphore Registers
- 256 Bytes of Dual-Port RAM
- Eight Address Lines
- Available in a 40-Pin Dual In-Line Package (DIP) or a 44-Pin Plastic Leaded Chip Carrier (PLCC)

Ordering Information

Package Type	Temperature Range	Frequency	Device
40-Pin DIP	0° C to +70° C	1.25 MHz	MC68HC34P
40-Pin DIP	– 40° C to +85° C	1.25 MHz	MC68HC34CP
40-Pin DIP	0° C to +70° C	2.0 MHz	MC68HCB34P
40-Pin DIP	– 40° C to +85° C	2.0 MHz	MC68HCB34CP
44-Pin PLCC	0° C to +70° C	2.0 MHz	MC68HCB34FN

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

© MOTOROLA INC., 1992

Replaces MCM68H34/D

www.DataSheet4U.com

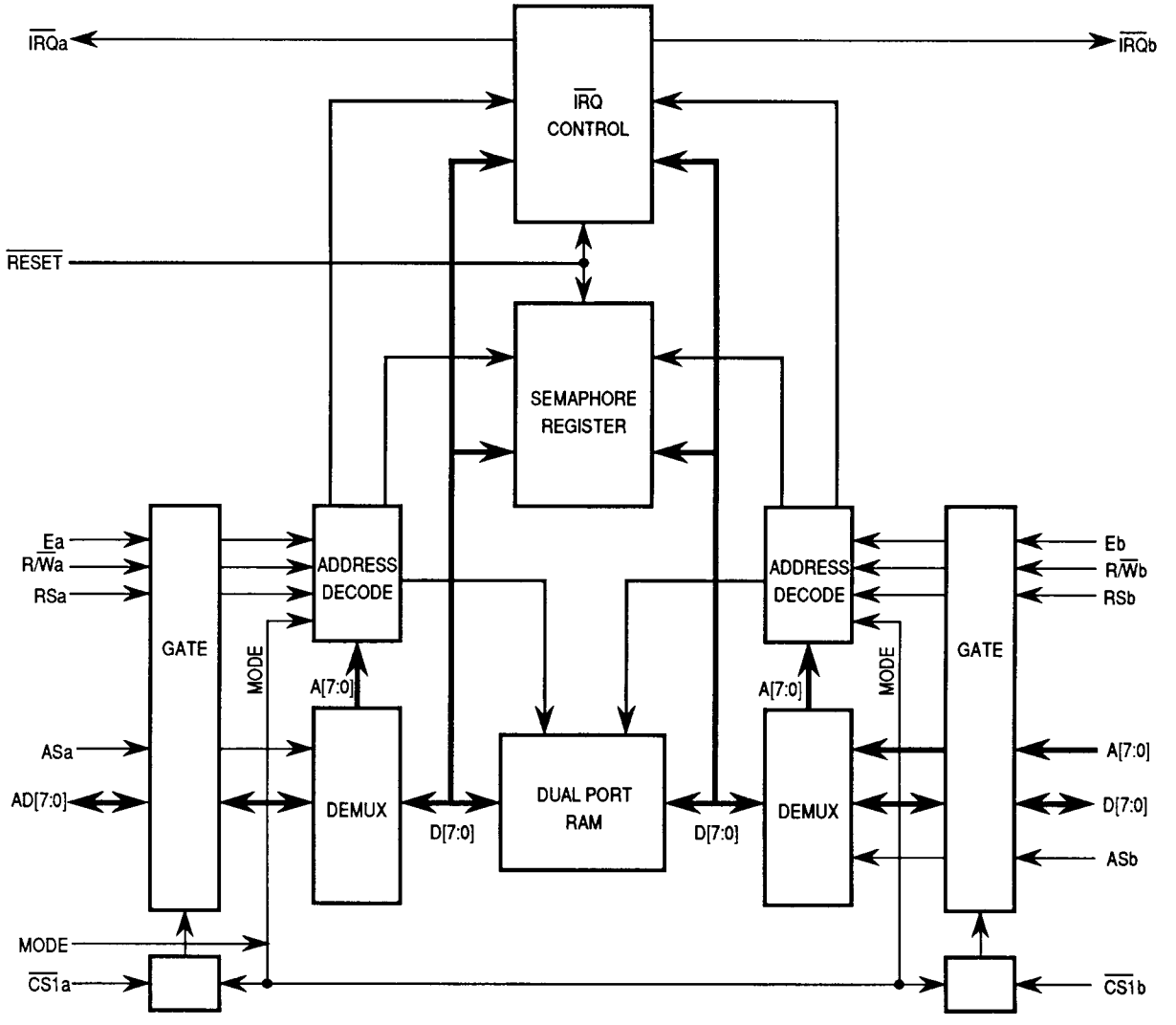
www.DataSheet4U.com

Table of Contents

Section **Page**

www.DataSheet4U.com

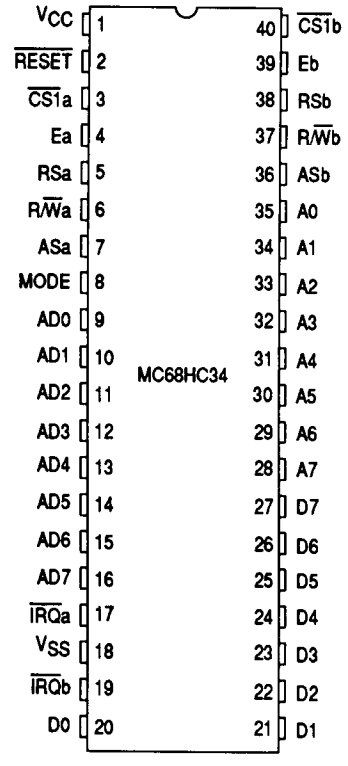
www.DataSheet4U.com



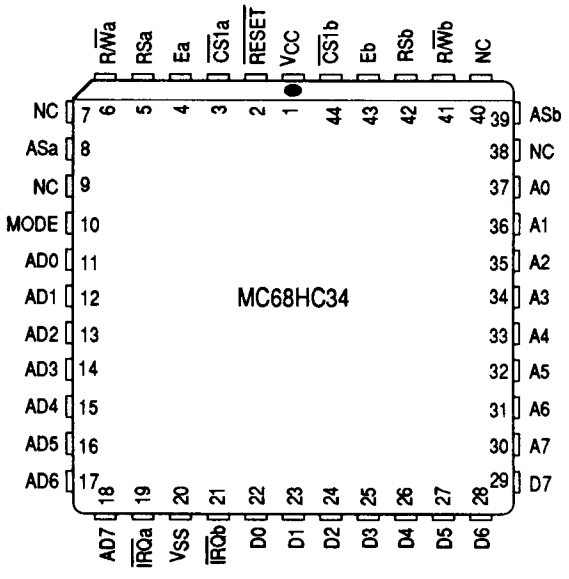
MC68HC34 Block Diagram

www.DataSheet4U.com

www.DataSheet4U.com



Pin Assignments for 40-Pin DIP (P suffix)



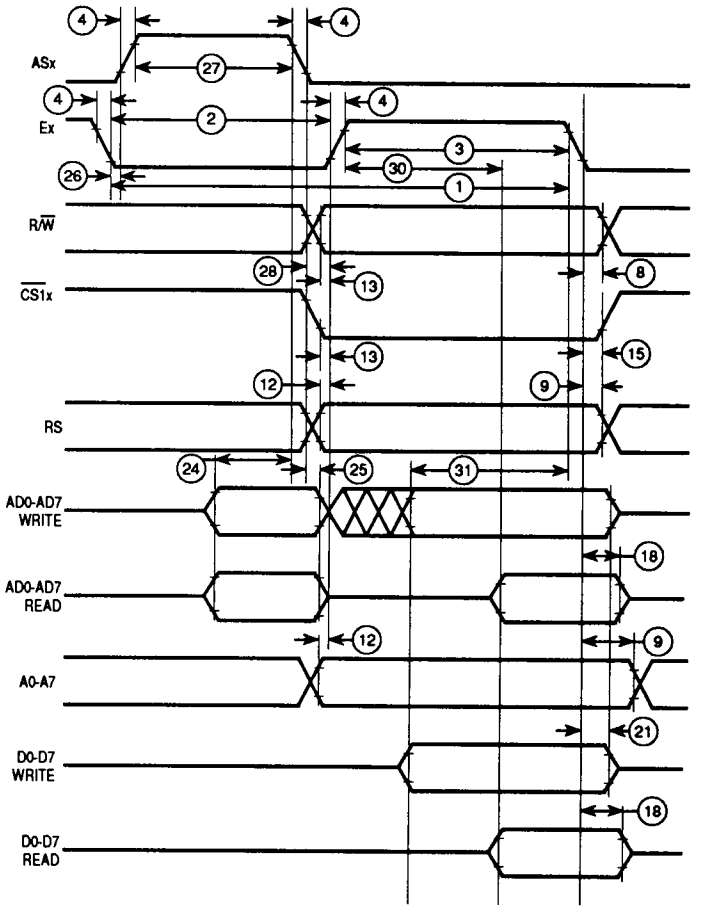
Pin Assignments for 44-Pin PLCC (FN suffix)

www.DataSheet4U.com

www.DataSheet4U.com

Bus Timing

The following diagram illustrates bus timing for the MC68HC34. The times referenced here are explained in detail in the table on the next page.



Bus Timing Diagram

www.DataSheet4U.com

www.DataSheet4U.com

This table describes the times referenced in the bus timing diagram on the previous page.

Bus Timing

Ident	Characteristics	Symbols	1.25 MHz (Standard)		2.0 MHz (B Speed)		Unit
			Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	800	–	500	–	ns
2	Pulse Width, E Low	P_{WEL}	300	–	220	–	ns
3	Pulse Width, E High	P_{WEH}	320	–	210	–	ns
4	Input Rise and Fall Time	t_r, t_f	–	30	–	20	ns
8	Read/Write Hold Time	t_{RWH}	10	–	10	–	ns
9	Nonmultiplexed Address, RS Hold Time	t_{AH}	10	–	10	–	ns
12	Nonmultiplexed Address, RS Valid Time to Eb	t_{AV}	20	–	20	–	ns
13	Read/Write, Chip-Select Setup Time	t_{RWS}	20	–	20	–	ns
15	Chip-Select Hold Time	t_{CH}	0	–	0	–	ns
18	Read Data Hold Time	t_{DHR}	20	75	10	75	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	ns
24	Address Setup Time for Latch	t_{ASL}	20	–	20	–	ns
25	Address Hold Time for Latch	t_{AHL}	20	–	20	–	ns
26	Delay Time E to AS Rise	t_{ASD}	60	–	50	–	ns
27	Pulse Width, AS High	PW_{ASH}	110	–	50	–	ns
28	Address Strobe to E Delay	t_{ASED}	20	–	20	–	ns
30	Read Data Delay Time (Access Time)	t_{DDR}	–	240	–	180	ns
31	Write Data Setup Time	t_{DSW}	100	–	80	–	ns

NOTES:

1. Timing numbers relative to one side only. No numbers are intended to be cross-referenced from one side to the other.
2. Measurement points for AC timing are 0.8 V and 2.5 V, unless otherwise specified.

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	– 0.3 to 7.0	V
Input Voltage	V_{in}	V_{SS} – 0.3 to V_{CC} + 0.5	V
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	– 55 to 150	°C

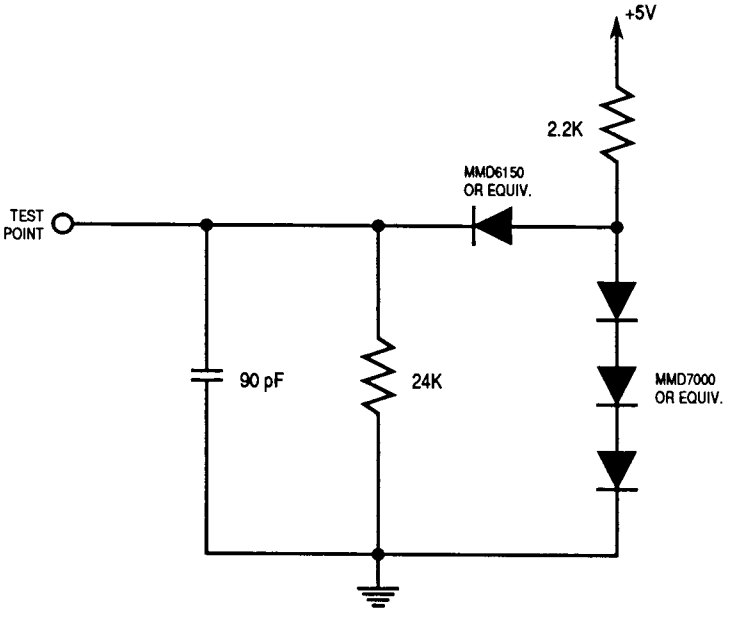
www.DataSheet4U.com

www.DataSheet4U.com

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this high-impedance circuit. Unused inputs must be tied to an appropriate logic level (either V_{CC} or V_{SS}) to reduce leakage currents and to increase reliability.

Thermal Charactistics

Characteristic	Symbol	Value	Unit
Thermal Resistance			
Plastic DIP (P suffix)	θ_{JA}	100	°C/W
PLCC (FN suffix)	θ_{JA}	60	°C/W



Bus Timing Load

www.DataSheet4U.com

www.DataSheet4U.com

DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input High Voltage (See note 1.)	V_{IH}	2.5	V_{CC} + 0.3	V
Input High Voltage, "C" Temp. Range (See note 1.)	V_{IH}	2.75	V_{CC} + 0.3	V
Input Low Voltage (See note 2.)	V_{IL}	V_{SS} – 0.3	0.8	V
Input Current (V_{in} = 0 to V_{CC})	I_{in}	–	1.0	µA
Output Leakage Current	I_{OZ}	–	10.0	µA
Output High Voltage (I_{Load} = – 100 µA)	V_{OH}	2.4	–	V
(I_{Load} ≤ 100 µA)		V_{CC} – 0.1	–	
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	–	0.4	V
(I_{Load} ≤ 10.0 µA)		–	0.1	
Current Drain – Outputs Unloaded Operating – Ea, Eb = 1 MHz, Both Sides Active	I_{DD}	–	30	mA
Input Capacitance	C_{in}	–	10	pF
Output Capacitance AD[7:0] and D[7:0]	C_{out}	–	12	pF

NOTES:

1. Input high voltage as stated is for all inputs except MODE. In the case of MODE, input high voltage is tied to V_{CC}.
2. Input low voltage as stated is for all inputs except MODE. In the case of MODE, input low voltage is tied to V_{SS} or is floating. If floating, the voltage will be internally pulled to V_{SS}.

Signal Description

V_{CC} and V_{SS}

These pins supply power to the DPM. V_{CC} is + 5 volts ± 5% and V_{SS} is 0 volts or ground.

Ea and Eb

These are the E clock inputs from processor A and processor B, respectively and are positive during the latter portion of the bus cycle.

RSa and RSb

Register inputs RSa and RSb control the selection of either the semaphore and interrupt registers or the 256 bytes of RAM. A high on RSa or RSb allows selection of the semaphore and interrupt registers for side A or side B by the lower three of the upper four address bits. A low on input RSa or RSb selects the 256 bytes of RAM for side A or side B.

www.DataSheet4U.com

www.DataSheet4U.com

$\overline{CS1a}$ and $\overline{CS1b}$

$\overline{CS1a}$ and $\overline{CS1b}$ are chip-select inputs for side A and side B respectively. When $\overline{CS1a}$ or $\overline{CS1b}$ is low, either side A or side B is selected. If $\overline{CS1a}$ or $\overline{CS1b}$ is high, either side A or side B is deselected.

MODE

In normal operation the mode select pin should always be connected to V_{CC} (MODE = 1). Each side has three states controlled by RSa and $\overline{CS1a}$ for side A and RSb and $\overline{CS1b}$ for side B.

If $\overline{CS1a}$ is low, side A accesses either 256 bytes of RAM or the six semaphore registers and the two interrupt registers depending on the level of RSa. If $\overline{CS1a}$ is high, side A cannot access the DPM. If RSa is low, 256 bytes of RAM are accessed, and if RSa is high, the semaphore and the two interrupt registers are accessed.

The six semaphore and two interrupt registers are redundantly mapped in the 256-byte mode. That is, only the low order three bits select one of the eight registers and the upper five bits of address are not decoded. Refer to the following table.

Side A Control Signal Operation

Mode	$\overline{CS1a}$	RSa	Operation
1	0	0	Access 256 bytes RAM Side A
1	0	1	Access Semaphore/$\overline{IRQ}$ Side A on Lower Three of Upper Four Bits of Address
1	1	X	Side A Not Selected

The three states for side B in the 256 byte mode are controlled in the same manner as side A using $\overline{CS1b}$ and RSb except that side B uses separate address and data inputs. Refer to the following table.

Side B Control Signal Operation

Mode	$\overline{CS1a}$	RSb	Operation
1	0	0	Access 256 bytes RAM Side B
1	0	1	Access Semaphore/$\overline{IRQ}$ Side B on Lower Three of Upper Four Bits of Address
1	1	X	Side B Not Selected

$\overline{IRQa}$ and $\overline{IRQb}$

Interrupt request signals ($\overline{IRQa}$ and $\overline{IRQb}$) are active low open-drain outputs. A write by processor A to address F9 clears RSb and, if not masked on side B, interrupts processor B. A write by processor B to address F9 clears RSa and, if not masked on side A, interrupts processor A.

www.DataSheet4U.com

www.DataSheet4U.com

A[7:0] and D[7:0]

A[7:0] refer to the address bus inputs for side B. D[7:0] are the directional data bus pins for side B. When side B is run from a multiplexed bus processor, the side B address pins are connected to the corresponding side B data pins (A0 to D0, A1 to D1, etc.).

$\overline{\text{Reset}}$

A low level on this input causes the semaphore registers to be set to the states shown in the table titled Reset State of Semaphore Registers and clears both bits of both $\overline{\text{IRQ}}$ registers. The RAM data is unaffected by $\overline{\text{RESET}}$.

ASa and ASb

ASa and ASb are the address strobe inputs for the A side and the B side, respectively. The ASa input demultiplexes the eight low order address bits from the data lines on the A side. The falling edge of ASa latches the A side address within the DPM. The ASb input is used in the same manner when the B side is connected to a multiplexed bus. The ASb input must be connected to a high level when the B side is connected to a nonmultiplexed bus.

AD[7:0]

AD[7:0] are the multiplexed address/bidirectional data bus inputs for the A side of the DPM. The A side can only be used with a multiplexed address/data bus. The A side addresses are on these lines during the time ASa is high. The lines are used as bidirectional data lines during the time Ea is high.

Dual-Port RAM

The DPM contains 256 bytes of dual-port RAM that is accessed from either processor. It is selected in either case by eight address lines, register and chip-select inputs. The direction of data transfer is controlled by the respective read/write (R/$\overline{\text{W}}$a or R/$\overline{\text{W}}$b) line.

Simultaneous accesses by both processors of different locations of dual-port RAM will cause no ambiguities. Simultaneous reads of the same RAM location gives the proper data to both sides. Simultaneous write and simultaneous write and read to the same location should be avoided for two reasons. Simultaneous writes to the same RAM location result in undefined data being stored. On a simultaneous write and read of the same location, the data written is put into RAM but the data read is undefined. The semaphore registers provide the tool for determining when the shared RAM is available.

Semaphore Registers

The DPM contains six read/write semaphore registers. Only two bits of each register are used. Bit 7 is the semaphore (SEM) bit and bit 6 is the ownership (OWN) bit. The remaining six bits all read zeros.

Each semaphore register is able to arbitrate simultaneous accesses by both processors. The semaphore register bits provide a mechanism for controlling accesses to the shared RAM but there are no hardware controls of the dual-port RAM by the semaphore registers.

www.DataSheet4U.com

www.DataSheet4U.com

Below is the truth table for a semaphore register when it is accessed by one of the processors. When a semaphore register is written, the actual data written is disregarded but the SEM bit is cleared. When a semaphore register is read the resulting SEM bit is one. If a zero is read the processor sees the resource as available but leaves a one to tell the other processor that the resource is busy. When the data is written the bit is cleared (ready for another read). If a one is read, that processor sees the resource as busy but leaves a one in case it tries to access the resource again before the other processor clears the SEM bit.

Single Processor Semaphore Bit Truth Table

Original SEM Bit	R/$\overline{W}$	Data Read	Resulting SEM Bit
0	R	0*	1
1	R	1*	1
0	$\overline{W}$	—	0
1	$\overline{W}$	—	0

* 0 = Resource Available
* 1 = Resource Not Available

Below is the truth table if both processors read or read and write the same semaphore register at the same time. The A processor always reads the actual SEM bit. The B processor reads the SEM bit except during the simultaneous read of a clear SEM bit. This ensures that during a simultaneous read, only the A processor reads a clear SEM bit and therefore has priority to the shared RAM.

Simultaneous Access of Semaphore Register Truth Table

Original SEM Bit	A Processor		B Processor		Resulting SEM Bit
	R/$\overline{W}$	Data Read	R/$\overline{W}$	Data Read	
0	R	0*	R	1*	1
1	R	1*	$\overline{W}$	—	0
1	$\overline{W}$	—	R	1*	0
1	R	1*	R	1*	1

* 0 = Resource Available
* 1 = Resource Not Available

The ownership bit is a read-only bit that indicates which processor last set the SEM bit. The OWN bit is set whenever the SEM bit is set. The OWN bit as read by one processor is the complement of the bit read by the other processor.

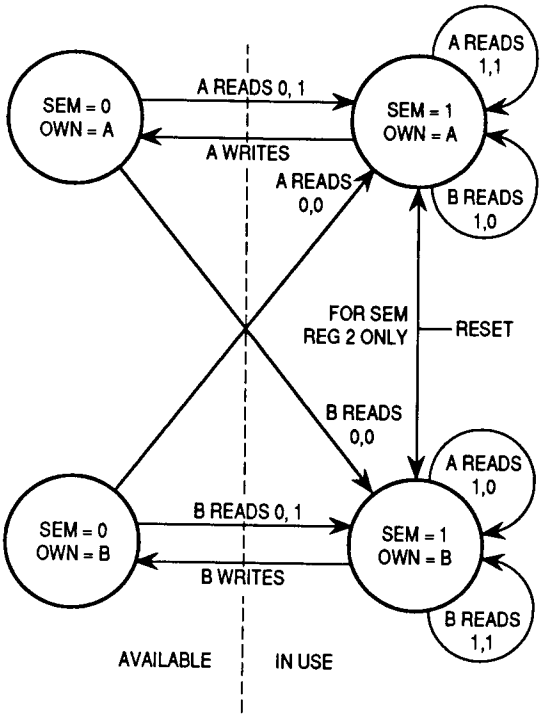
www.DataSheet4U.com

www.DataSheet4U.com

The reset state of the semaphore registers is defined in the following table. The A side processor owns all of the semaphore registers except the second semaphore register which is owned by the B side processor.

Reset State of Semaphore Registers

Semaphore Register	A Processor		B Processor	
	SEM Bit	OWN Bit	SEM Bit	OWN Bit
1	1	1	1	0
2	1	0	1	1
3	1	1	1	0
4	1	1	1	0
5	1	1	1	0
6	1	1	1	0



State Diagram for a Semaphore Register

NOTE

Writes to a semaphore register are valid only if SEM = 1 and OWN = 1. When A and B simultaneously read a semaphore register, the hardware handles it as a read by A followed by a read by B.

www.DataSheet4U.com

www.DataSheet4U.com

Interrupt Registers

The DPM contains two addressable locations at F8 and F9 on both sides that control the interrupt (IRQ) operation between the two processors. Although there is only one hardware register for each side, for purposes of explanation, the register location accessed at F8 is referred to as the IRQx status register and the register accessed at location F9 is referred to as the IRQx control register (refer to the IRQ Registers table). The registers each consist of two bits and have identical bit arrangements. Bit 6 is the enable bit and bit 7 is the flag bit. The other six bits are not used and always read as zero. When $\overline{\text{RESET}}$ is asserted both bits are cleared.

IRQ Registers

Location	Register Name	Bit 7	Bit 6	Bits 5 to 0
A Side F8	IRQa Status	Flag	Enable	Not Used
A Side F9	IRQa Control	Flag	Enable	Not Used
B Side F8	IRQb Status	Flag	Enable	Not Used
B Side F9	IRQb Control	Flag	Enable	Not Used

The Interrupt Operation table summarizes the bits involved when reading or writing to the status or control registers as F8 or F9. The enable bits on either side (A or B) track the data that is written into the status register from that side. Writes to the control register do not alter data. The actual data written is disregarded but the action sets the flag bit to the other side's register and asserts an interrupt signal if enabled.

Interrupt Operation

Operation	Action Taken
A Reads IRQa Status at F8	Read EA and FA
A Writes IRQa Status at F8	Writes EA
A Reads IRQa Control at F9	Read EA and FA; Clear FA
A Writes IRQa Control at F9	Set FB; Assert IRQb if Enabled
A Reads IRQb Status at F8	Read EB and FB
A Writes IRQb Status at F8	Writes to EB
A Reads IRQb Control at F9	Read EB and FB; Clear FB
A Writes IRQb Control at F9	Set FA; Assert IRQa if Enabled

NOTES:

1. F8 and F9 are address locations.
2. EA and FA are side A enable and flag bits.
3. EB and FB are side B enable and flag bits.

www.DataSheet4U.com

www.DataSheet4U.com

When the enable bit in the IRQb status register is set (bit 6 = 1), a write to IRQa control register sets the flag bit in the IRQb status register (bit 7 = 1) and causes an interrupt on the B side (IRQb pin = low). Reading the IRQb status register reads the state of the B side enable and flag bits. Reading the IRQb control register also reads the enable and flag bits but clears the B side flag bit (bit 7 = 0) and clears the B side interrupt by removing the low condition on the IRQb pin. The A side interrupt is controlled in a similar manner.

The enable bit in the IRQb status register is changed by writing the proper data to bit 6 of the IRQb status register. If the B side enable bit is zero, interrupts on the B side are prevented. However, a write to the IRQa control register still sets the B side flag bit.

Internal Register Addresses

The Register Locations table shows the address of the RAM, IRQ, and semaphore registers. The addresses to these registers are the same whether accessed from the A side or the B side. The address and data buses are multiplexed on the A side. The B side has separate address and data buses. The B side can be used on a multiplexed bus by connecting the corresponding address and data pins together (A0 to D0, A1 to D1, etc.) and using the B side address strobe input (ASb).

Register Locations

RS	Address	Register Name
0	00 – FF	Dual-Port RAM
1	X0 – X7	IRQ and Semaphore
1	X8 – XF	IRQ and Semaphore

NOTES:

1. In the above table, X represents 0 through F.
2. Oniy the lower three of the upper four bits of each register are decoded.
3. When RS is high, the address contains the semaphore and IRQ registers and is redundantly mapped throughout the RAM.

www.DataSheet4U.com